Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 73462

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 — VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008/2010)

(Also common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the various issues in Technology-CAD
2. Define the lambda layout rules.
3. List out the limitations of the constant voltage scaling.
4. Draw the small signal model of a MOSFET.
5. Implement a 2:1 Multiplexer using pass transistor.
6. Design a 1-bit dynamic register using pass transistor.
7. Define boundary scan test.
8. What are the stages at which a chip can be tested?
9. State the operators used in Verilog HDL.
10. Write a Verilog program for a CMOS inverter using switch level modelling.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the electrical properties of MOS transistor in detail.

Or

(b) Derive an expression for V_{in} of a CMOS inverter to achieve the condition $V_{in} = V_{out}$. What should be the relation for $\beta_n = \beta_p$.

12. (a) (i) Explain in detail about the scaling concept and reliability concept. (8)

(ii) Describe in detail about the transistor sizing for the performance in combinational networks. (8)

Or

(b) Discuss in detail about the resistive and capacitive delay estimation of a CMOS inverter circuit. (16)

13. (a) (i) Describe the different methods of reducing static and dynamic power dissipation in CMOS circuits. (8)

(ii) Explain the domino and dual rail domino logic families with neat diagrams. (8)

Or

(b) (i) Draw and explain the operation of conventional CMOS, pulsed and resettable latches. (8)

(ii) Write a brief note on sequencing dynamic circuits. (8)

14. (a) Briefly discuss the following terms: (16)

(i) Testers

(ii) Test fixtures

(iii) Test programs.

Or

(b) (i) Explain the Silicon debug principles in detail. (8)

(ii) Explain the Manufacturing test principles in detail. (8)

15. (a) Explain how to represent the gate delays in Verilog HDL with an example.

Or

(b) (i) Write a Verilog code for D-flip-flop. (8)

(ii) Explain blocking and non-blocking assignments. (8)